National Semiconductor

September 1996

DS90C032 LVDS Quad CMOS Differential Line Receiver

General Description

The DS90C032 is a quad CMOS differential line receiver designed for applications requiring ultra low power dissipation and high data rates. The device is designed to support data rates in excess of 155.5 Mbps (77.7 MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The DS90C032 accepts low voltage (350 mV) differential input signals and translates them to CMOS (TTL compatible) output levels. The receiver supports a TRI-STATE® function that may be used to multiplex outputs. The receiver also supports OPEN, shorted and terminated (100Ω) input Failsafe. Receiver output will be High for all failsafe conditions.

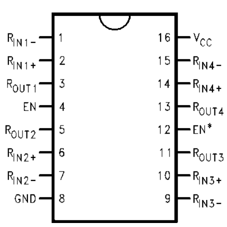
The DS90C032 and companion line driver (DS90C031) provide a new alternative to high power psuedo-ECL devices for high speed point to point interface applications.

Features

- >155.5 Mbps (77.7 MHz) switching rates
- Accepts small swing (350 mV) differential signal levels
- Ultra low power dissipation
- 600 ps maximum differential skew (5V, 25°C)
- 6.0 ns maximum propagation delay
- Industrial operating temperature range
- Military operating temperature range option
- Available in surface mount packaging (SOIC) and (LCC)
- Pin compatible with DS26C32A, MB570 (PECL) and 41LF (PECL)
- Supports OPEN, short and terminated input failsafe
- Compatible with IEEE 1596.3 SCI LVDS standard
- Conforms to ANSI/TIA/EIA-644 LVDS standard
- Available to Standard Microcircuit Drawing (SMD) 5962-96834

Connection Diagrams

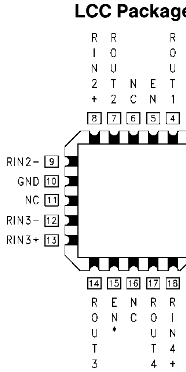
Dual-In-Line



TL/F/11945–1

Order Number DS90C032TM
See NS Package Number M16A

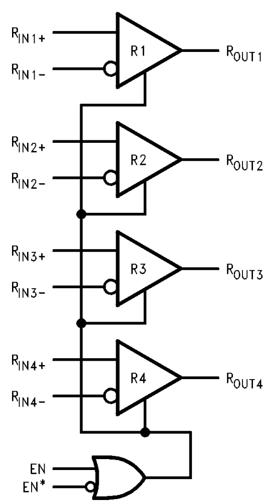
LCC Package



TL/F/11945–20

Order Number DS90C032E-QML
See NS Package Number E20A

Functional Diagram and Truth Tables



TL/F/11945–2

RECEIVER

ENABLES		INPUTS	OUTPUT
EN	**EN***	$R_{IN+} - R_{IN-}$	R_{OUT}
L	H	X	Z
All other combinations of ENABLE inputs		$V_{ID} \geq 0.1V$	H
		$V_{ID} \leq -0.1V$	L
		Full Failsafe OPEN/SHORT or Terminated	H

For complete Military Specifications, see SMD.

TRI-STATE® is a registered trademark of National Semiconductor Corporation.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +6V
Input Voltage (RIN+, RIN−)	−0.3V to (V_{CC} +0.3V)
Enable Input Voltage (EN, EN*)	−0.3V to (V_{CC} +0.3V)
Output Voltage (ROUT)	−0.3V to (V_{CC} +0.3V)
Maximum Package Power Dissipation @ +25°C	
M Package	1025 mW
E Package	1830 mW
Derate M Package	8.2 mW/°C above +25°C
Derate E Package	12.2 mW/°C above +25°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range Soldering (4 sec.)	+260°C
Maximum Junction Temperature (DS90C032T)	+150°C
Maximum Junction Temperature (DS90C032E)	+175°C
ESD Rating (HBM 1.5 kΩ, 100 pF)	≥ 3,500V (Note 7)

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	+4.5	+5.0	+5.5	V
Receiver Input Voltage	GND		2.4	V
Operating Free Air Temperature (T_A)				
DS90C032T	−40	+25	+85	°C
DS90C032E	−55	+25	+125	°C

Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (Note 2).

Symbol	Parameter	Conditions		Pin	Min	Typ	Max	Units
V_{TH}	Differential Input High Threshold	V_{CM} = +1.2V		R_{IN}+, R_{IN}−			+100	mV
V_{TL}	Differential Input Low Threshold				−100			mV
I_{IN}	Input Current	V_{IN} = +2.4V	V_{CC} = 5.5V		−10	±1	+10	μA
		V_{IN} = 0V			−10	±1	+10	μA
V_{OH}	Output High Voltage	I_{OH} = −0.4 mA, V_{ID} = +200 mV		R_{OUT}	3.8	4.9		V
		I_{OH} = −0.4 mA, Input terminated	DS90C032T		3.8	4.9		V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA, V_{ID} = −200 mV				0.07	0.3	V
I_{OS}	Output Short Circuit Current	Enabled, V_{OUT} = 0V (Note 8)			−15	−60	−100	mA
I_{OZ}	Output TRI-STATE Current	Disabled, V_{OUT} = 0V or V_{CC}			−10	±1	+10	μA
V_{IH}	Input High Voltage			EN, EN*	2.0			V
V_{IL}	Input Low Voltage						0.8	V
I_I	Input Current				−10	±1	+10	μA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−1.5	−0.8		V
I_{CC}	No Load Supply Current	EN, EN* = V_{CC} or GND, Inputs Open	DS90C032T	V_{CC}		3.5	10	mA
			DS90C032E			3.5	11	mA
	Receivers Enabled	EN, EN* = 2.4 or 0.5, Inputs Open				3.7	11	mA
I_{CCZ}	No Load Supply Current	EN = GND, EN* = V_{CC}	DS90C032T			3.5	10	mA
	Receivers Disabled	Inputs Open	DS90C032E			3.5	11	mA

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (Notes 3–5, 9) DS90C032T

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHLD}	Differential Propagation Delay High to Low	C_L = 5 pF V_{ID} = 200 mV (*Figures 1* and *2*)	1.5	3.40	5.0	ns
t_{PLHD}	Differential Propagation Delay Low to High		1.5	3.48	5.0	ns
t_{SKD}	Differential Skew $\|t_{PHLD} - t_{PLHD}\|$		0	80	600	ps
t_{SK1}	Channel to Channel Skew	(Note 5)	0	0.6	1.0	ns
t_{TLH}	Rise Time	(*Figures 1* and *2*)		0.5	2.0	ns
t_{THL}	Fall Time			0.5	2.0	ns
t_{PHZ}	Disable Time High to Z	(*Figures 3* and *4*)		10	15	ns
t_{PLZ}	Disable Time Low to Z			10	15	ns
t_{PZH}	Enable Time Z to High			4	10	ns
t_{PZL}	Enable Time Z to Low			4	10	ns

Switching Characteristics

V_{CC} = +5.0V ± 10%, T_A = −40°C to +85°C (Notes 3–6, 9) DS90C032T

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHLD}	Differential Propagation Delay High to Low	C_L = 5 pF V_{ID} = 200 mV (*Figures 1* and *2*)	1.0	3.40	6.0	ns
t_{PLHD}	Differential Propagation Delay Low to High		1.0	3.48	6.0	ns
t_{SKD}	Differential Skew $\|t_{PHLD} - t_{PLHD}\|$		0	0.08	1.2	ns
t_{SK1}	Channel to Channel Skew	(Note 5)	0	0.6	1.5	ns
t_{SK2}	Chip to Chip Skew	(Note 6)			5.0	ns
t_{TLH}	Rise Time	(*Figures 1* and *2*)		0.5	2.5	ns
t_{THL}	Fall Time			0.5	2.5	ns
t_{PHZ}	Disable Time High to Z	(*Figures 3* and *4*)		10	20	ns
t_{PLZ}	Disable Time Low to Z			10	20	ns
t_{PZH}	Enable Time Z to High			4	15	ns
t_{PZL}	Enable Time Z to Low			4	15	ns

Switching Characteristics

V_{CC} = +5.0V ± 10%, T_A = −55°C to +125°C (Notes 3–6, 9) DS90C032E

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHLD}	Differential Propagation Delay High to Low	C_L = 20 pF V_{ID} = 200 mV *(Figures 1* and *2)* (Note 10)	1.0	3.40	8.0	ns
t_{PLHD}	Differential Propagation Delay Low to High		1.0	3.48	8.0	ns
t_{SKD}	Differential Skew $\|t_{PHLD} - t_{PLHD}\|$		0	0.08	3.0	ns
t_{SK1}	Channel to Channel Skew	(Note 5)	0	0.6	3.0	ns
t_{SK2}	Chip to Chip Skew	(Note 6)			7.0	ns
t_{PHZ}	Disable Time High to Z	*(Figures 3* and *4)*		10	20	ns
t_{PLZ}	Disable Time Low to Z			10	20	ns
t_{PZH}	Enable Time Z to High			4	20	ns
t_{PZL}	Enable Time Z to Low			4	20	ns

Parameter Measurement Information

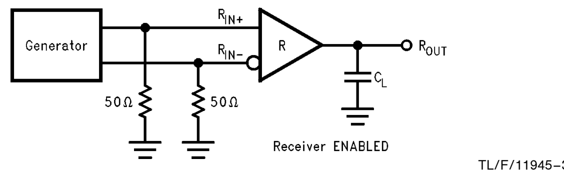


FIGURE 1. Receiver Propagation Delay and Transition Time Test Circuit

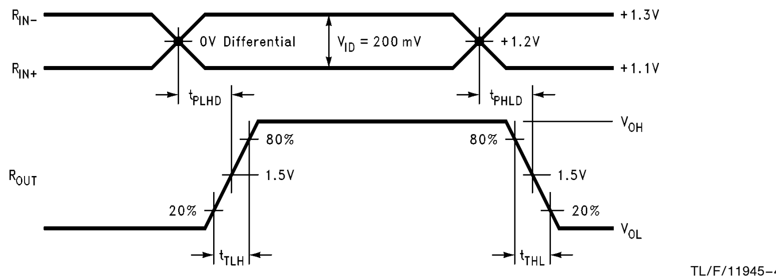
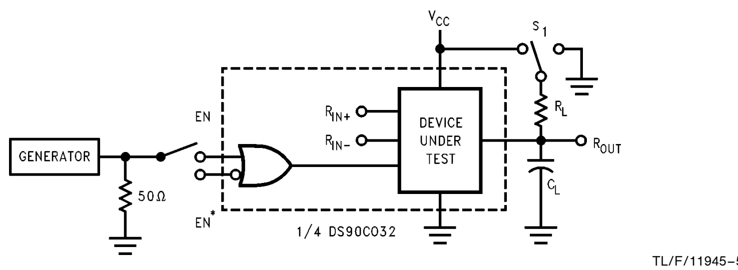


FIGURE 2. Receiver Propagation Delay and Transition Time Waveforms



C_L includes load and test jig capacitance.
S_1 = V_{CC} for t_{PZL}, and t_{PLZ} measurements.
S_1 = GND for t_{PZH} and t_{PHZ} measurements.

FIGURE 3. Receiver TRI-STATE Delay Test Circuit

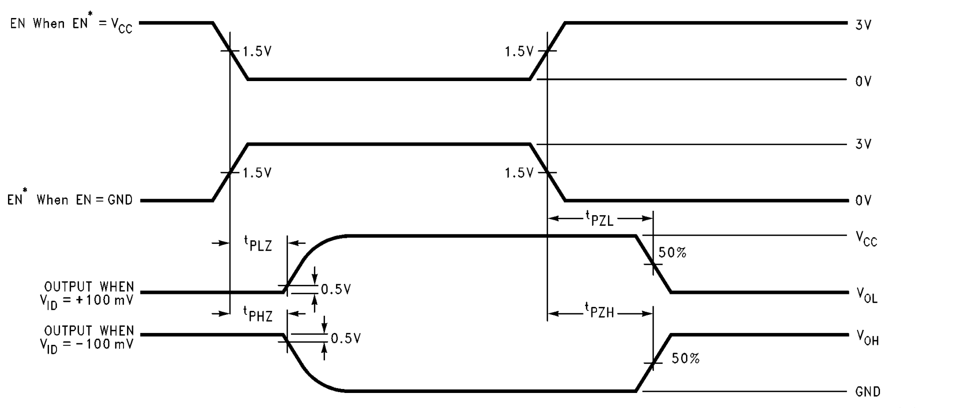


FIGURE 4. Receiver TRI-STATE Delay Waveforms

Typical Application

Balanced System

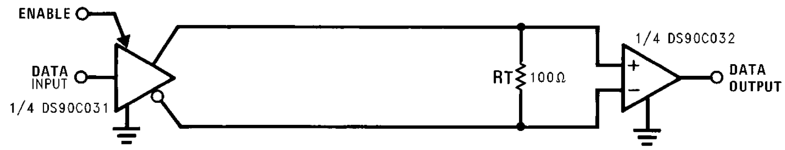


FIGURE 5. Point-to-Point Application

Applications Information

LVDS drivers and receivers are intended to be primarily used in an uncomplicated point-to-point configuration as is shown in *Figure 5.* This configuration provides a clean signaling environment for the quick edge rates of the drivers. The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically the characteristic impedance of the media is in the range of 100Ω. A termination resistor of 100Ω should be selected to match the media, and is located as close to the receiver input pins as possible. The termination resistor converts the current sourced by the driver into a voltage that is detected by the receiver. Other configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities as well as ground shifting, noise margin limits, and total termination loading must be taken into account.

The DS90C032 differential line receiver is capable of detecting signals as low as 100 mV, over a ±1V common mode range centered around +1.2V. This is related to the driver offset voltage which is typically +1.2V. The driven signal is centered around this voltage and may shift ±1V around this center point. The ±1V shifting may be the result of a ground potential difference between the driver's ground reference and the receiver's ground reference, the common mode effects of coupled noise, or a combination of the two. Both receiver input pins should honor their specified operating input voltage range of 0V to +2.4V (measured from each pin to ground), exceeding these limits may turn on the ESD protection circuitry which will clamp the bus voltages.

The receiver also supports a failsafe feature which provides a stable (known state) high output voltage for any of the following conditions:

1. **Open Input Pins.** The DS90C032 is a quad receiver device, and if an application requires only 1, 2 or 3 receivers, the unused channel(s) inputs should be left OPEN. Do not tie unused receiver inputs to ground or other voltages. The internal circuitry will guarantee a high, stable output state.
2. **Terminated Input.** If the driver is in a TRI-STATE condition, or if the driver is in a power-off condition, or if the driver is even disconnected (cable unplugged), the receiver output will again be in a high state, even with the end of cable 100Ω termination resistor across the input pins.
3. **Shorted Inputs.** If a cable fault condition occurs that shorts the twisted pair conductors together, thus resulting in a 0V differential input voltage to the receiver, the receiver output will remain in a high state.

The footprint of the DS90C032 is the same as the industry standard 26LS32 Quad Differential (RS-422) Receiver.

Pin Descriptions

Pin No. (SOIC)	Name	Description
2, 6, 10, 14	$R_{IN}+$	Non-inverting receiver input pin
1, 7, 9, 15	$R_{IN}-$	Inverting receiver input pin
3, 5, 11, 13	R_{OUT}	Receiver output pin
4	EN	Active high enable pin, OR-ed with EN*
12	EN*	Active low enable pin, OR-ed with EN
16	V_{CC}	Power supply pin, +5V ±10%
8	GND	Ground pin

Ordering Information

Operating Temperature	Package Type/ Number	Order Number
−40°C to +85°C	SOP/M16A	DS90C032TM
−55°C to +125°C	LCC/E20A	DS90C032E-QML
DS90C032E-QML (NSID) 5962-96834 (SMD)		

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.

Note 3: All typicals are given for: $V_{CC} = +5.0V$, $T_A = +25°C$.

Note 4: Generator waveform for all tests unless otherwise specified: f = 1 MHz, $Z_O = 50\Omega$, t_r and t_f (0%–100%) ≤ 1 ns for R_{IN} and t_r and t_f ≤ 6 ns for EN or EN*.

Note 5: Channel to Channel Skew is defined as the difference between the propagation delay of one channel and that of the others on the same chip with an event on the inputs.

Note 6: Chip to Chip Skew is defined as the difference between the minimum and maximum specified differential propagation delays.

Note 7: ESD Rating: HBM (1.5 kΩ, 100 pF) ≥ 3,500V
EIAJ (0Ω, 200 pF) ≥ 250V

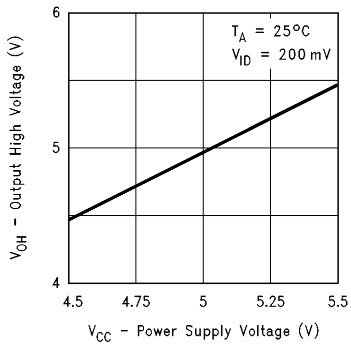
Note 8: Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only. Only one output should be shorted at a time, do not exceed maximum junction temperature specification.

Note 9: C_L includes probe and jig capacitance.

Note 10: For DS90C032E propagation delay measurements are from 0V on the input waveform to the 50% point on the output (R_{OUT}).

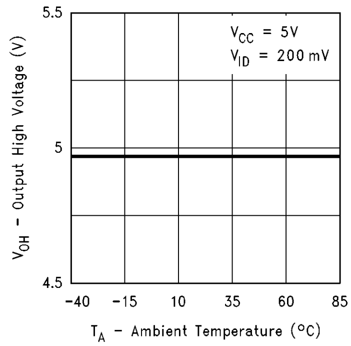
Typical Performance Characteristics

Output High Voltage vs Power Supply Voltage



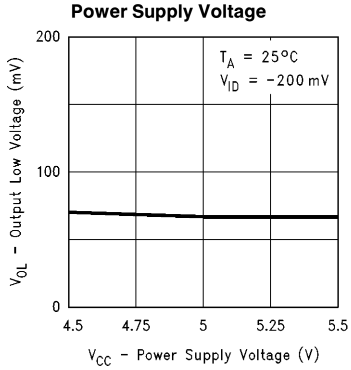
TL/F/11945–8

Output High Voltage vs Ambient Temperature



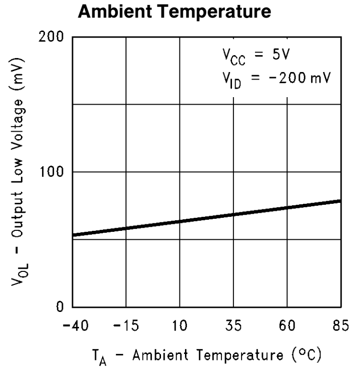
TL/F/11945–9

Output Low Voltage vs Power Supply Voltage



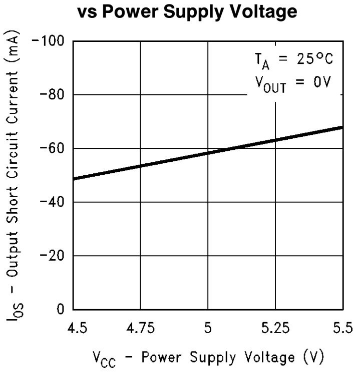
TL/F/11945–10

Output Low Voltage vs Ambient Temperature



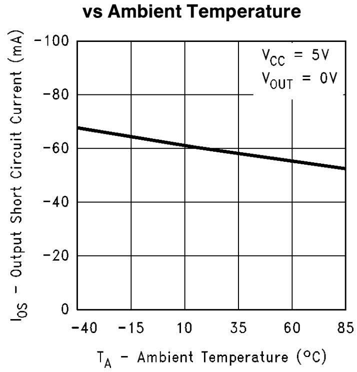
TL/F/11945–11

Output Short Circuit Current vs Power Supply Voltage



TL/F/11945–12

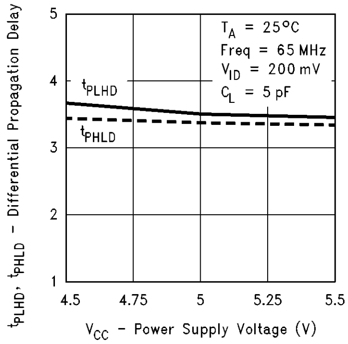
Output Short Circuit Current vs Ambient Temperature



TL/F/11945–13

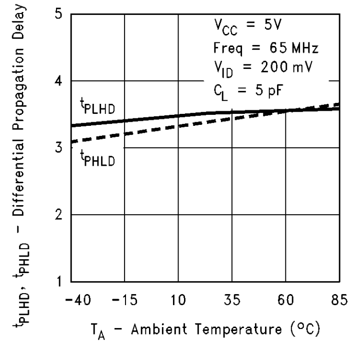
Typical Performance Characteristics (Continued)

Differential Propagation Delay vs Power Supply Voltage



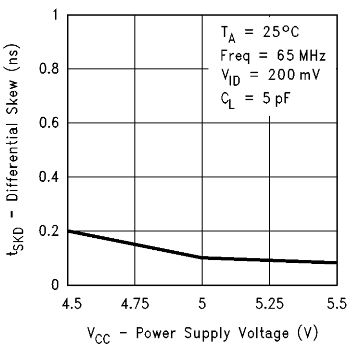
TL/F/11945–14

Differential Propagation Delay vs Ambient Temperature



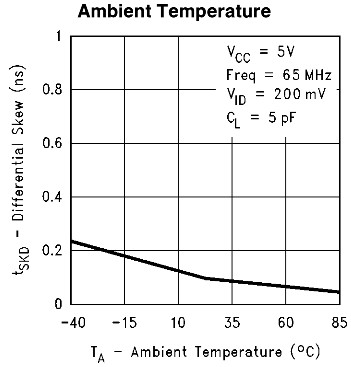
TL/F/11945–15

Differential Skew vs Power Supply Voltage



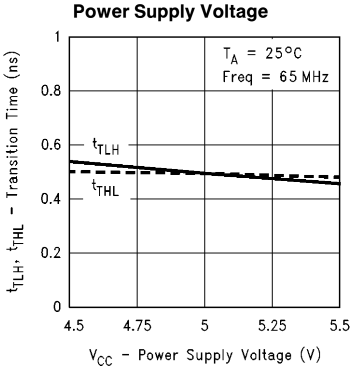
TL/F/11945–16

Differential Skew vs Ambient Temperature



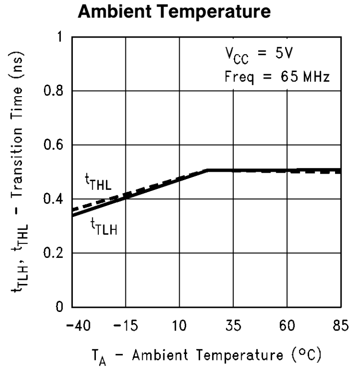
TL/F/11945–17

Transition Time vs Power Supply Voltage



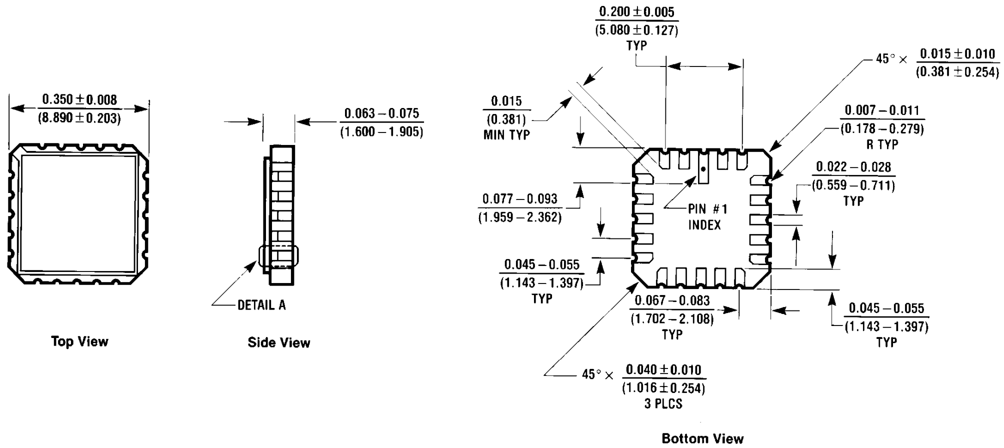
TL/F/11945–18

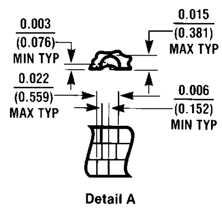
Transition Time vs Ambient Temperature



TL/F/11945–19

Physical Dimensions inches (millimeters) unless otherwise noted

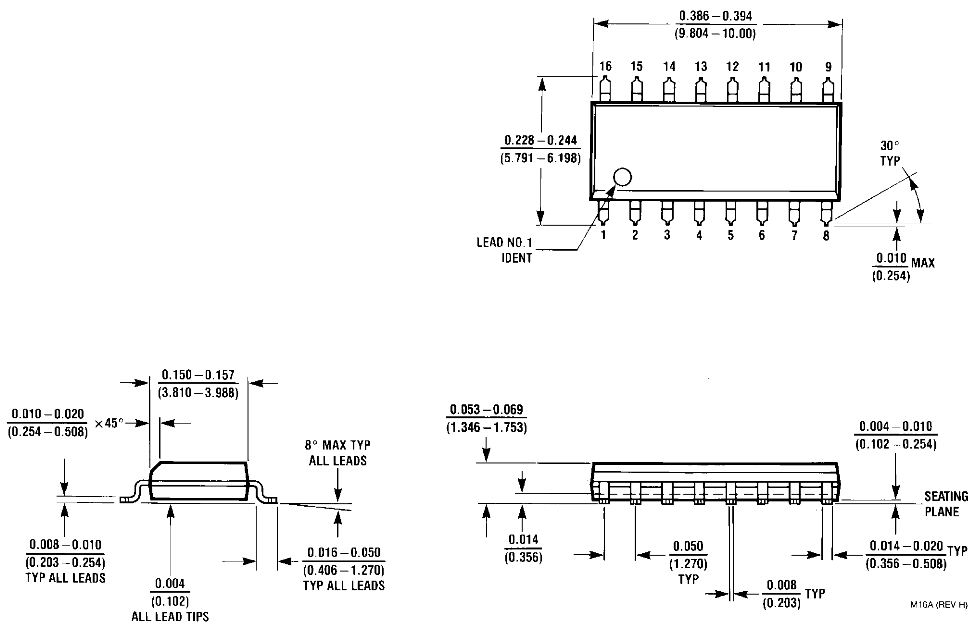




E20A (REV D)

20-Lead Ceramic Leadless Chip Carrier, Type C
Order Number DS90C032E-QML
NS Package Number E20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead (0.150″ Wide) Molded Small Outline Package, JEDEC
Order Number DS90C032TM
NS Package Number M16A

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

http://www.national.com

National Semiconductor Europe
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 180-530 85 85
English Tel: +49 (0) 180-532 78 32
Français Tel: +49 (0) 180-532 93 58
Italiano Tel: +49 (0) 180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2308
Fax: 81-043-299-2408